# Neutral Interconnections and Kirchhoff's Laws 

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#### Abstract

We show that, for an electrical circuit made up of two-terminal components, Kirchhoff's laws imply that the interconnection of the components is a neutral interconnection in a control theory sense.


## 1. Introduction

It is generally agreed that control theory and electrical circuit theory have a lot in common, and certainly some insights have been shared between those two subject areas. There is, however, a difference in approach when talking about connections between subsystems. In the language of control theory one talks of inputs and outputs, and an interconnection is what happens when the outputs of some subsystems are connected to the inputs of other subsystems. In circuits, inputs and outputs are not clearly defined, and interconnections happen when nodes are connected to other nodes. The concept of a "node" does not map easily into control theory terms.

The constraints on interconnections of circuit components are Kirchhoff's laws, and it is hard to express those without mentioning nodes and loops.

In this paper we look for a way of expressing an equivalent of Kirchhoff's laws in terms of inputs and outputs. The individual components in a circuit will almost be ignored, because the focus is on the interconnections.

## 2. Neutral interconnections

The notion of a neutral interconnection was introduced in [3]. The basic idea is that an interconnection of dissipative subsystems is called a neutral interconnection if the dissipativeness parameters of the interconnected system are the same as those of the original collection of subsystems.

Suppose we have a number of subsystems that are $(Q, S, R)$ dissipative in the sense

$$
\left\langle y_{i}, Q_{i} y_{i}\right\rangle_{T}+2\left\langle y_{i}, S_{i} u_{i}\right\rangle_{T}+\left\langle u_{i}, R_{i} u_{i}\right\rangle_{T} \geq 0
$$

for all $i$ and all $u_{i}$, assuming that each subsystem is initially at rest, where the subscript $T$ is the causal truncation operator, and $u_{i}$ and $y_{i}$ are the input and output, respectively. Let $u$ and $y$ be vectors formed by stacking up the individual inputs and outputs. Then

$$
\langle y, Q y\rangle_{T}+2\langle y, S u\rangle_{T}+\langle u, R u\rangle_{T} \geq 0
$$

where $Q=$ block $\operatorname{diag}\left\{Q_{1}, Q_{2}, Q_{3}, \ldots\right\}$, and similarly for $S$ and $R$. That is, the collection of subsystems, with no interconnection between them, is $(Q, S, R)$ dissipative.
Now let those subsystems be interconnected via the equation

$$
u=u_{\text {ext }}-H y
$$

where $H$ is a constant matrix, and $u_{\text {ext }}$ is a vector of external inputs. A short calculation shows that

$$
\langle y, \hat{Q} y\rangle_{T}+2\left\langle y, \hat{S} u_{e x t}\right\rangle_{T}+\left\langle u_{e x t}, \hat{R} u_{e x t}\right\rangle_{T} \geq 0
$$

where

$$
\begin{gathered}
\hat{Q}=Q-S H-H^{T} S^{T}+H^{T} R H \\
\hat{S}=S-H^{T} R \\
\hat{R}=R
\end{gathered}
$$

We call the interconnection neutral if $(\hat{Q}, \hat{S}, \widehat{R})=(Q, S, R)$. Clearly the necessary and sufficient conditions for this to be true are $H^{T} R=0$ and $S H+H^{T} S^{T}=0$.

The special case of passivity is of special interest. In that case the connection is neutral iff $H+H^{T}=0$. For a neutral interconnection in the passivity sense, the overall system is passive when all the subsystems are passive. Examples of neutral interconnections, in the passivity sense, are systems connected in parallel, and single-loop feedback.
Intuitively, an interconnection described by Kirchhoff's laws should be a neutral interconnection, because it is an interconnection that preserves passivity. (See Tellegen's theorem in Section 4.) The aim of this paper is to explore that question, and specifically to find a way of expressing Kirchhoff's laws as a feedback equation.

## 3. Circuits as interconnections

In control theory, an interconnection is a connection from the outputs of subsystems to the inputs of other subsystems. In circuit theory, the components (subsystems) are connected at nodes, and the rules controlling those connections are Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL). Our goal in this paper is to ask whether Kirchhoff's laws are more or less restrictive than the rules described in the last section, and to find a form of Kirchhoff's laws that can be expressed as connections from outputs to inputs.

Each component, a two-terminal object, has a voltage $v_{k}$ and a current $i_{k}$, and the relationship between them is the constitutive relation of that component. The selection of the reference directions of currents and voltages is largely arbitrary, but in what follows we will require that the directions be compatible in the following sense: the reference direction for current always flows from the + terminal to the - terminal, with those signs determining the reference direction for voltage. This is the normal convention for passive components. It is the opposite of what is normally assumed for sources, but this will not be a problem.


For simplicity we consider only two-terminal components, but the extension to multiterminal components requires only minor changes of notation. A transistor, for example, has three terminals, but the voltage and current relations as seen from outside the
transistor still obey Kirchhoff's laws. A transformer is commonly treated as two or more twoterminal components, one for each winding. It is true that there are interdependencies between the windings, but those interrelationships occur only in the constitutive relations. They do not change how Kirchhoff's laws apply.
A complete circuit can be viewed as a graph, with a component (a subsystem) in each branch. The constitutive relations govern what happens in each branch, and KCL and KVL describe the interconnections. But can we describe the interconnections in terms of inputs and outputs?

For a single component we can say that the input is the current and the output is the voltage, or vice versa. If the relationship between voltage and current is invertible, we can choose either as the input. We can hit a complication in the case of some nonlinear circuits. With a tunnel diode, for example, we can express the current as a function of voltage, but the voltage cannot be expressed as a single-valued function of current. This restriction is fundamental: for some circuit components, there is no choice over which of the two variables should be called the input.

Even without that problem, it is not clear how to express interconnections in terms of inputs and outputs. Circuit theory relies heavily on the concept of nodes, for which there is nothing comparable in input-output descriptions. Certainly we can consider each element to be a oneport network, but the only obvious "port" interpretations are for series and parallel connections of one-ports.
For deriving state equations we can extract the capacitors and inductors [1], leaving a multiport resistor. This, however, does not go as far as looking at how the resistive components are interconnected.
Working in terms of two-ports is a little more promising. The following circuit can be thought of as a connection of four two-port circuits and one one-port capacitor, where the dotted lines show the separation between the subsystems.


The port equations are easy to write down. A shunt resistor, for example, has port equations

$$
\left[\begin{array}{l}
v_{2} \\
i_{2}
\end{array}\right]=\left[\begin{array}{cc}
1 & 0 \\
1 / R & -1
\end{array}\right]\left[\begin{array}{l}
v_{1} \\
i_{1}
\end{array}\right]
$$

and the connections between the ports are easily interpreted as connections from outputs to inputs.
This approach works well for ladder circuits, for parallel subcircuits, and a few other cases, but it is not sufficiently general. It is impossible, for example, to put a bridge circuit into this form.

## 4. Tellegen's theorem

Let $A$ be a matrix with entries

$$
A_{i j}=\left\{\begin{aligned}
+1 & \text { if } i_{j} \text { flows into node } i \\
-1 & \text { if } i_{j} \text { flows out of node } i \\
0 & \text { otherwise }
\end{aligned}\right.
$$

(We will need this definition again in Section 7.) Then it is easy to see that KCL becomes

$$
A i=0
$$

A row of $A$ can contain several nonzero entries, because several branches can be connected to a node. It is not hard to see, however, that each column may only contain two non-zero entries, one with value +1 and the other with value -1 , because column $j$ corresponds to branch $j$.

KVL is automatically satisfied if we assign a voltage, with respect to an arbitrarily chosen reference node, to each node. Let $v_{\text {node }}$ denote the vector of node voltages. Every branch voltage is the difference between two node voltages, and in fact the relevant two nodes are identified by the columns of $A$. With a suitable numbering of the nodes, the vector $v$ of branch voltages is given by

$$
v=A^{T} v_{\text {node }}
$$

From this it easily follows that

$$
v^{T} i=v_{\text {node }}^{T} A i=0
$$

This is the simplest form of Tellegen's theorem [4]. It says that the sum of the powers consumed by the branches is zero. If we let one or more of those branches be ports, then the sum of the powers into the ports is equal to the sum of powers consumed by the non-port branches. (To see this, you have to observe that the current sign convention for a port is the opposite of that which we have adopted for the branches.) This implies, among other things, that an N -port made from passive components is itself passive.

The complete statement of Tellegen's theory is more flexible, because it allows the currents and voltages to be measured under different conditions, but we don't need that version here.
Although this is an elegant result, it is not quite what we need to pose the property in control theory terms. The method of proof does make it clear that this is about connections, with no reference to component properties, and this is a step towards what we want. It does, however, rely on the concept of "node voltage", for which there is no good parallel in an input-output model.

## 5. Tie-sets

If one writes out the KCL equation at every node in a circuit, and the KVL equation for every loop, the result will be a lot of redundant equations. Two standard ways of going directly to a minimal set of equations are called cut-set analysis and tie-set analysis. In this section we will look at the tie-set approach. This is standard material [2], but needs to be described here because the topic appears to have disappeared from most modern texts.

Consider a circuit as a graph. (That is, we are identifying the nodes and branches, without needing to look at what components are in the branches.) A spanning tree of the graph is a subgraph that includes all nodes, but has no loops. The ties, also called links, are the branches that had to be removed to break the loops.
The example at right shows, first the graph of a circuit with six nodes and nine branches, and then a spanning tree for that graph. The spanning tree is shown in bold, and the links as dotted lines. In what follows, we need the branches and links to be numbered, and to have a
 reference direction for every branch and link. (To reduce confusion, the links in this example have been "numbered" with the letters $\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{d}$.) The numbering and the assignment of directions are both completely arbitrary, but once the choice has been made we must remain consistent.

It is important to understand that this is only one of the possible spanning trees. Several other choices would have been possible.

Restoring one link to the tree creates exactly one loop, so we can say that each link defines a loop in the graph. Let us number the loops with the link numbers.

We can divide the circuit currents into two groups. Let $i_{\text {link }}$ be a vector of link currents, and let $i_{b r}$ be a vector of the remaining branch currents: the currents in the spanning tree. It does not matter how we number the branches, as long as we are consistent from this point on. Similarly, let $v_{\text {link }}$ be a vector of link voltages, and let $v_{b r}$ be a vector of spanning tree branch voltages.
Each spanning tree branch current is the superposition of one or more loop currents; that is, the sum of one or more link currents. Using this approach, KCL is automatically satisfied. Define a matrix $B$ by

$$
B_{j k}=\left\{\begin{array}{cl}
+1 & \text { if branch } j \text { is in loop } k \text {, with the same orientation }  \tag{1}\\
-1 & \text { if branch } j \text { is in loop } k \text {, with the opposite orientation } \\
0 & \text { otherwise }
\end{array}\right.
$$

Then that superposition can be expressed by

$$
i_{b r}=B i_{l i n k}
$$

Now, each column of $B$ describes the path along one loop, so $B^{T} v_{b r}$ is the sum of voltages around the loop, not including the link that closes the loop. Adding in the link voltages, KVL for all loops is

$$
v_{l i n k}+B^{T} v_{b r}=0
$$

These equations are for a circuit with no external ports. To test for (external) passivity, we can create a port by breaking a link and insert a voltage source in the opposite direction from the reference direction for that link. Alternatively, we can add a current source parallel to one of the branches in the spanning tree, again in the opposite direction from the reference
direction. To be sure that the circuit is externally passive no matter where we create the port, we can add these "probe" sources in every possible branch. The above equations then become

$$
\begin{gathered}
i_{b r}-i_{\text {ext }}=B i_{\text {link }} \\
\left(v_{\text {link }}-v_{\text {ext }}\right)+B^{T} v_{b r}=0
\end{gathered}
$$

where the $i_{\text {ext }}$ and $v_{\text {ext }}$ are the external sources.
Now define

$$
u_{\text {ext }}=\left[\begin{array}{l}
v_{\text {ext }} \\
i_{\text {ext }}
\end{array}\right] \quad \text { and } \quad u=\left[\begin{array}{c}
v_{\text {link }} \\
i_{b r}
\end{array}\right] \quad \text { and } \quad y=\left[\begin{array}{c}
i_{\text {link }} \\
v_{b r}
\end{array}\right]
$$

The equations now become

$$
\left[\begin{array}{c}
v_{\text {link }} \\
i_{b r}
\end{array}\right]=\left[\begin{array}{c}
v_{\text {ext }} \\
i_{\text {ext }}
\end{array}\right]-\left[\begin{array}{cc}
0 & B^{T} \\
-B & 0
\end{array}\right]\left[\begin{array}{c}
i_{\text {link }} \\
v_{b r}
\end{array}\right]
$$

or

$$
u=u_{\text {ext }}-H y
$$

where $H+H^{T}=0$. That is, we have finally put the Kirchhoff law equations into an inputoutput form, and indeed the connection turns out to be a neutral interconnection in the sense of Section 2.

## 6. Cut-sets

Given a connected graph, a cut-set is a set of branches which, if removed, would separate the network into two disconnected parts.

One way to form cut-sets is to start with a spanning tree. If we require the cut-set to include exactly one branch of the spanning tree, it can be seen that this specifies uniquely the set of links that must also be included in the cut-set. Thus, each branch in the spanning tree defines one cutset. For convenience we can use the branch number as the cutset number.

Define a matrix $C$ by

$$
C_{i j}=\left\{\begin{array}{cl}
+1 & \text { if link } j \text { is in cutset } i, \text { with the same orientation } \\
-1 & \text { if link } j \text { is in cutset } i, \text { with the opposite orientation } \\
0 & \text { otherwise }
\end{array}\right.
$$

Since a cutset divides the circuit into two parts, the sum of currents in a cutset must be zero.

$$
i_{b r}+C i_{l i n k}=0
$$

Recall that, in the last section, we expressed the spanning tree branch currents as the superposition of link currents. It is clear that there is only one such combination of link currents, which implies that $C=-B$. Thus, apart from the sign, the cutset matrix is the same as the tieset matrix, even though they were derived by different reasoning.
The difference between the cut-set and tie-set approaches lies in the choice of independent variables. In the tie-set case we start with the link currents, and express the KVL equations in terms of the link currents. In the cut-set case we start with tree branch voltages, and then write down an equivalent to the KCL equations. That difference, however, shows up only when we use the constitutive relations of the individual elements. If we focus only on the
interconnection equations, there is no difference between the two methods, and we are left with the previously derived equation

$$
\left[\begin{array}{c}
v_{\text {link }}  \tag{2}\\
i_{b r}
\end{array}\right]=\left[\begin{array}{c}
v_{\text {ext }} \\
i_{\text {ext }}
\end{array}\right]-\left[\begin{array}{cc}
0 & B^{T} \\
-B & 0
\end{array}\right]\left[\begin{array}{c}
i_{\text {link }} \\
v_{b r}
\end{array}\right]
$$

which is in the form

$$
u=u_{e x t}-H y
$$

Note that there are usually many possible spanning trees, and therefore many different ways of choosing the inputs and outputs, each of which will lead to a different $B$ matrix. Every such analysis will, however, still produce the property $H+H^{T}=0$, the defining property of a neutral interconnection.

## 7. The converse result

We have shown that Kirchhoff's laws imply equation (2). For completeness, we should ask whether equation (2) implies Kirchhoff's laws.

For a completely arbitrary $B$, the answer is obviously no. Since the variables in (2) are tree branches and links, it is implied that a spanning tree has already been chosen, and that means that $B$ should be precisely the matrix in (1) that describes the topological detail: the relationship between tree branches and loops.

In what follows we have no need of the external inputs, so we can set them all to zero. That leaves us with

$$
\begin{aligned}
v_{l i n k} & =-B^{T} v_{b r} \\
i_{b r} & =B i_{l i n k}
\end{aligned}
$$

For convenience, let us call the loops formed by the links the "basic loops". The first of these equations says that KVL is obeyed around all the basic loops. We now have to ask whether KVL is also true around every other closed path.

For closed paths that do not traverse any link, the result is trivially true. Any path that remains inside the tree can get back to its starting point only by retracing its outward path in the opposite direction. That means that the voltage drops along the way cancel each other out, for a final voltage drop of zero.

For all other paths, it is sufficient to show that we can assign a node voltage (with respect to some reference) to every node, without contradictions. If that can be shown, then KVL must be satisfied for all possible paths through the graph.

To assign node voltages, begin by choosing any basic loop. Select any node in that loop as the reference node, with a node voltage of zero, and then assign node voltages to the other nodes in that loop by adding or subtracting branch voltages while going around the loop. Because KVL is satisfied around a basic loop, the result will be back to zero by the time we get back to the starting point. That means that the node voltages along that path have been consistently assigned.

Then work through the remaining basic loops. For each such loop, there are three possibilities:
(a) All nodes in the loop have already been assigned node voltages. In this case, we can skip this loop and pass on to the next.
(b) None of the nodes in the loop have been assigned node voltages. That is, this loop has no nodes in common with previously considered loops. Put this loop on the back of the queue of loops still to be processed, and pass on to the next loop. We will come back to this loop later.
(c) Some but not all of the nodes in the loop have been assigned node voltages. Traverse the loop, assigning node voltages to the nodes not yet processed. Again, the results will be consistent because KVL holds around this loop.

In most cases this will result in node voltages being assigned to all nodes, in which case KVL must hold along all possible closed paths. There are, however, some pathological cases that can arise.

First, it can happen that we are left with some unused basic loops that have no nodes in common with the nodes already dealt with. That breaks the nodes into two groups, where no basic loop crosses between the groups. This can happen if the circuit is really two or more separate circuits. The only other way it can happen is if there is a cutset consisting of one tree branch and no links. In either case, we can continue assigning node voltages by treating the disconnected part as a separate circuit.
The second pathological case is where some nodes are left over after considering all basic loops. Those nodes cannot be part of any closed path apart from the tree-only paths that retrace their steps, and we have already shown that KVL holds for those paths.
Proving KCL is a little easier. Since we want to look at all currents, not separated into tree branches and links, define

$$
i=\left[\begin{array}{c}
i_{\text {branch }} \\
i_{\text {link }}
\end{array}\right]=\left[\begin{array}{c}
B \\
I
\end{array}\right] i_{\text {link }} \triangleq \widehat{B} i_{\text {link }}
$$

Now we want to reintroduce the matrix $A$, connecting branches and nodes, that was used in the proof of Tellegen's theorem. Specifically, we want to look at the product $A \widehat{B}$.

$$
(A \widehat{B})_{n k}=\sum_{m} A_{n m} \hat{B}_{m k}
$$

where $n$ is a node number, $k$ is a loop number, and the sum is over all elements $m$ in the loop. If node $n$ is not in loop $k$, every term in this sum will be zero. If loop $k$ does include node $n$, the sum will have exactly two nonzero terms

$$
(A \widehat{B})_{n k}=A_{n m_{1}} \hat{B}_{m_{1} k}+A_{n m_{2}} \hat{B}_{m_{2} k}
$$

where element $m_{1}$ is the element encountered just before node $n$, and $m_{2}$ is the one just after, as we traverse loop $k$. Each factor has value +1 or -1 . The signs of the $\hat{B}$ entries depends on the orientation of the element relative to the loop direction, and the signs of the $A$ entries depends on the orientation of the element relative to the node. On looking at all four pairs of orientations, it is easily seen that

$$
A_{n m_{2}} \hat{B}_{m_{2} k}=-A_{n m_{1}} \hat{B}_{m_{1} k}
$$

and therefore the sum is again zero. This means

$$
\begin{gathered}
A \widehat{B}=0 \\
A i=A \widehat{B} i_{\text {link }}=0
\end{gathered}
$$

Recall from Section 4 that the equation $A i=0$ is precisely the statement of KCL.

## 8. Conclusions

The goal in this paper was to express the interconnection between components in a multicomponent circuit in terms of inputs and outputs. The answer turns out to lie in using a spanning tree of the circuit graph. Once a tree is chosen, the inputs are the link voltages and the tree currents, and the outputs are the link currents and the tree branch voltages.
Regardless of which tree is chosen, Kirchhoff's laws lead to an interconnection matrix which is a neutral interconnection in the sense of reference [3]. Conversely, the neutral interconnection equation implies Kirchhoff's laws.

## References

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